Senior Design Project in Electrical Engineering

FIELD RESPONSE EMERGENCY DEPLOYABLE

Differential Global Positioning System (DGPS) Evaluation & Analysis

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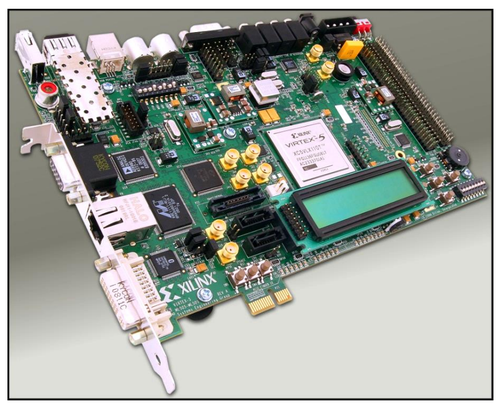
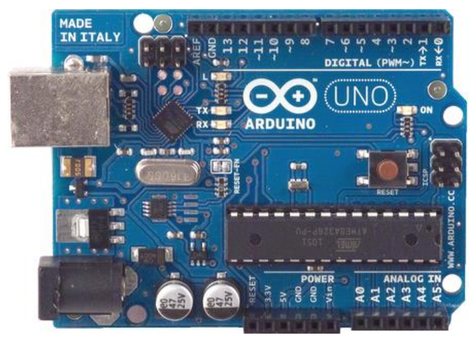
PROJECT BACKGROUND

The USCG maintains and operates the Differential Global Positioning System (DGPS). However, the Coast Guard lacks a government owned, non-proprietary way to test and validate DGPS stations in the field. The Field Response Emergency Deployable (FRED) project was developed to create an integrated and easily deployable system to test DGPS stations. The system uses a field programmable gate array (FPGA) to build a DGPS receiver that can receive and store message data and provide immediate assessment as well as detailed analysis. The use of an FPGA programmed with Verilog code provides a flexible and expandable system that can be tailored to meet future needs. A database stores the data received, a graphical user interface to allow simple use of the system with minimal training, and a microcontroller system which coordinates and communicates between the different modules.

Validation of DGPS can be essential in the wake of natural disasters such as Hurricane Katrina.



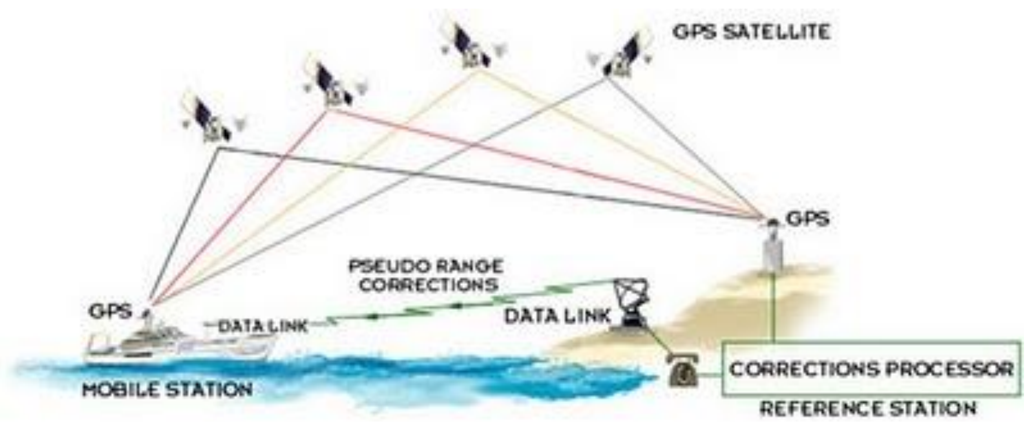


A field programmable gate array (FPGA) and Arduino microcontroller give the system additional flexibility.

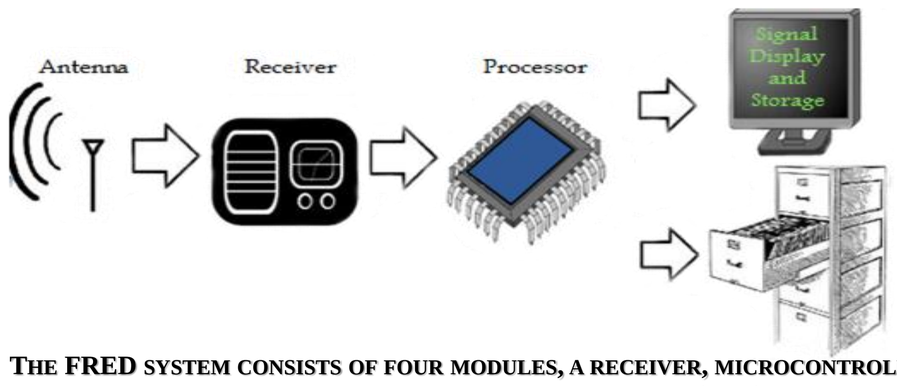
PROJECT REQUIREMENTS

Five major requirements were identified for the project:

- Easily transported for field deployment
- Receive, demodulate, and parse DGPS messages
- Provide two user levels: a basic "field" user and an advanced "engineer" user
- Store DGPS messages for advanced analysis
- Multi-channel capability



DGPS improves the accuracy of standard GPS by broadcasting local corrections to the GPS broadcast signals



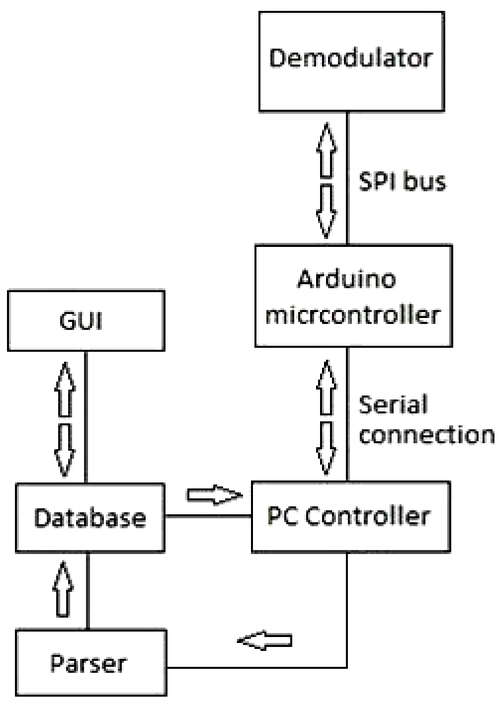
The FRED system consists of four modules, a receiver, microcontroller, database, and graphical user interface (GUI)

PROJECT DELIVERABLES

The project goals are as follows:

- Create a software-defined DGPS signal demodulator using an FPGA
- Create a DGPS receiver capable of receiving the entire spectrum of DGPS signals
- Create a parser that can decode and store the DGPS messages
- Create a system that is capable of analyzing the data for validity

COMMUNICATIONS DIAGRAM



RESULTS

The system consists of an active band pass filter to limit input to the 285 kHz – 325 kHz DGPS band combined with a commercial off the shelf amplifier to increase the input signal strength before passing it to an analog digital converter. A signal pre-processor within the FPGA super heterodyne receiver prepares the signal before it is demodulated using a matched filter. Communications are controlled by an Arduino microcontroller that connects to the FPGA via a serial peripheral interface (SPI) bus, extracts the demodulator output, and passes it to parser via a serial connection with the PC. The parser searches the demodulated data to locate the message preamble to determine if there is a valid DGPS message. When a preamble is located, the parser determines the validity of the message, parses the message components, and stores the data in the database.

FRONT-END FILTER/AMPLIFIER